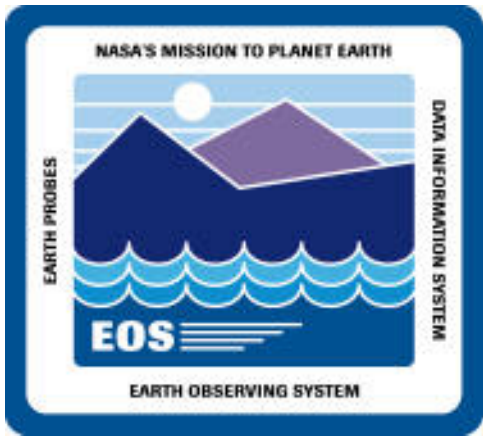

DAAC Hardware Designs

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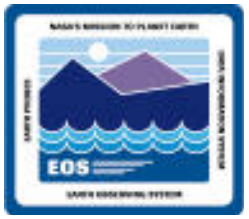
22 April 1996

Hardware Specification Methodology

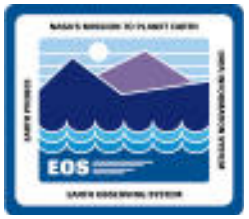


The system hardware specification process includes the following steps:

- **Gathering all requirements (includes performance modeling)**
- **Identifying all options and performing trade-offs**
- **Validating the specification**
- **Documenting the specification**

These steps are performed iteratively until solutions are found which optimally satisfy constraints

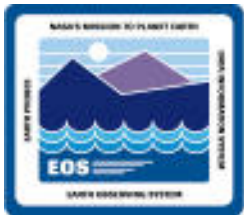
System Level Requirements



System Level Requirements may impact system hardware specification:

- **Performance ==> processing, I/O and memory must be selected to meet performance needs**
- **Phasing ==> hardware procurement must be phased to meet requirements**
- **RMA ==> may be met through implementation of failover pairs, sparing, use of replication techniques, etc.**
- **Scalability ==> must enable system growth without redesign (as specified in Level 3s for subsystems)**
- **Evolvability ==> must enable migration to new technologies**
- **Interoperability ==> may preclude the use of proprietary technologies**

Derived Requirements

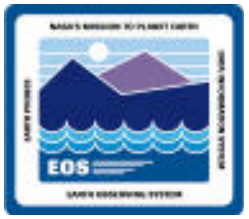


Requirements derived from modeling and/or benchmarking include:

- **Computing throughput (MIPS, MFLOPS)**
- **Random Access Memory (MB)**
- **Virtual Memory (MB)**
- **Network throughput (Mbps)**
- **Number of Robots**
- **Number of Read/Write Stations**
- **Disk Space (GB)**
- **Disk I/O (MB/sec)**

Inputs to modeling include the ECS Technical Baseline, vendor specifications, benchmark results, and analysis of custom software

Modeling / Sizing Approaches



The *Static Model* of AHWGP inputs provides coarse system sizing for production and data server systems.

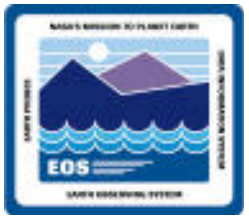
The *ECS Dynamic Model* simulates the work done to process and store ECS products. It provides significant detail about peak resource requirements.

***Subsystem-specific models* and analyses are used to derive details about requirements for specific configurations (e.g., specifics of the archive configuration).**

The *ECS End-to-End Model* is a queuing model used to analyze all ECS subsystems, using scenarios that take into consideration the system requirements and the candidate hardware design.

***Benchmarks/Prototypes* are used to measure the resource usage of COTS products and developed software as they will be used in the DAAC.**

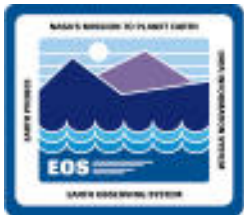
Hardware Configuration



For each subsystem, we will describe:

- **Computing platforms**
  - **Make, model, number of CPUs, expected capacity**
  - **I/O configuration (e.g., number of slots used)**
  - **Memory**
  - **Network attachment**
- **Storage (RAID, disk, tape libraries)**
  - **number and capacity of units**
  - **logical <-> physical mapping (e.g., placement of data to optimize use)**
- **Networks**
  - **protocols**
  - **selection of devices**
  - **topology, including security and addressing considerations**

Hardware Sizing / DAAC Designs Agenda



Introduction	**8:00 - 8:15**
Subsystem Hardware Designs	**8:15 - 10:30**
ORNL Hardware Design	**10:30 - 11:00**
NSIDC Hardware Design	**11:00 - 11:30**
JPL Hardware Design	**11:30 - 12:00**
SMC Hardware Design	**12:45 - 1:00**
GSFC Hardware Design	**1:00 - 1:30**
EDC Hardware Design	**1:30 - 2:00**
LaRC Hardware Design	**2:00 - 2:30**
ASF Hardware Design	**2:30 - 3:00**